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Nathaniel L. Bleier

Research Interests

I am interested in extending the reach of computing to new applications and domains whose constraints are not met by traditional computing platforms. My work has focused on architectures and chips for three such domains. First, I have designed and built computer chips in flexible electronics for applications with the conformality, thinness, and cost constraints that cannot be met by silicon chips. Second, I have designed novel architectures for earable and olfactory computing platforms that I believe will drive a large class of new and important computing applications in the future. Third, I design computer systems for in-space computing - I believe that space is going to be a new and increasingly important frontier of computing.

Publication Summary & Impact

- 6× (ISCA, MICRO), 3× (DAC, DATE)
- 1× ISCA Retrospective (1996-2020) Selection, 1× ISCA 50 Best Paper Award Nomination, 1× IEEE Top Picks Honorable Mention
- Property Driven Automatic Transformation tool (DAC 2021) licensed by ARM Research to reduce gate count in custom Cortex-M0 processor.
- Flexicores, plastic microprocessors with sub-cent cost (ISCA 2022), selected as a top semiconductor story for 2022 by IEEE Spectrum.

Chip Tape-Outs

- **O3 RISC-V Processor (Bring-up Pending)** 2023
  Design and tape-out of a performance oriented, dual-issue, out-of-order RISC-V core using explicit register renaming, and single-cycle misprediction recovery in Intel 16 nm *technology. The* 4 mm^2 *chip will be packaged with flip-chip packaging.*

- **High yield, field-programmable flexible microprocessors** 2022
  Three distinct flexible microprocessor designs using Pragmatic 0.8 µm *IGZO-TFT process implementing three distinct and custom instruction sets designed to enable expressivity and low gate count microarchitectures.*

- **RISC-V SoC** 2022
  An SoC consisting of a four-stage, single issue, in-order RISC-V core with split L1 caches, a high-throughput AES-128 accelerator, custom JTAG debug port, multiple SPI ports, external maskable and non-maskable interrupts, and 32 KiB *integrated data memory in* 65 nm *silicon technology.*

- **Flexible Encryption Accelerators** 2022
  Three flexible encryption accelerators for ISO standard cryptosystems (AES-128, PRESENT, and Simon) using Pragmatic 0.6 µm *IGZO-TFT process. The AES-128 implementation is, to the best of my knowledge, the lowest gate count implementation of an AES-128 accelerator to be manufactured.*

- **Printed Stochastic Computing Neural Network** 2021
  Neural network accelerators using unary stochastic computing. Networks were implemented with electrolyte gated FETs in full-custom logic designs.

- **Organic Pseudo-CMOS microprocessors (Bring-up Pending)** 2023
  A custom 8 bit *microprocessors made from organic thin-film transistors and implemented using pseudo-CMOS logic. These microprocessor have been fabricated and are awaiting testing.*

Service

- **HPCA — Program Committee Member** 2024
- **Education Justice Project** 2022–2023

  Work with individuals and groups of incarcerated people at Danville correctional facility to develop mathhematics and programming skills.
- **Warrior Leaders Project - Research Project Leader** 2021-2023

  Lead small groups of pre-undergraduate veterans in cryptanalysis of several cryptosystems, including polyalphabetic ciphers.
- **United States Army** 2008–2014

  Led small infantry units (30-120 men) in training and combat operations. Planned platoon, company, and battalion (≈ 600 soldier) level training and combat operations.

Publications

[1] **N. Bleier**, M. Mubarik, G. Swenson, and R. Kumar, "Space microdatacenters", in *MICRO '23*.

[2] **N. Bleier**, A. Wezelis, L. Varshney, and R. Kumar, "Programmable olfactory computing", in *ISCA '23*, **Best Paper Award Nominee**.

[3] **N. Bleier**, M. H. Mubarik, S. Balaji, F. Rodriguez, A. Sou, S. White, and R. Kumar, "Exploiting short application lifetimes for low cost hardware encryption in flexible electronics", in *DATE '23*.

[4] **N. Bleier**, M. H. Mubarik, S. Chakraborty, S. Kishore, and R. Kumar, "Rethinking programmable earable processors", in *ISCA '22*.

[5] **N. Bleier**, C. Lee, F. Rodriguez, A. Sou, S. White, and R. Kumar, "Flexicores: Low footprint, high yield, field reprogrammable flexible microprocessors", in *ISCA '22*, **Selected as a top semiconductor story of 2022 by IEEE Spectrum**.

[6] **N. Bleier**, J. Sartori, and R. Kumar, "Property-driven automatic generation of reduced-isa hardware", in *DAC '21*, **Licensed by ARM Research to reduce gate count in custom Cortex-M0 processor.**

[7] D. D. Weller, **N. Bleier**, M. Hefenbrock, J. Aghassi-Hagmann, M. Beigl, R. Kumar, and M. B. Tahoori, "Printed stochastic computing neural networks", in *DATE '21*.

[8] M. H. Mubarik, D. D. Weller, **N. Bleier**, M. Tomei, J. Aghassi-Hagmann, M. B. Tahoori, and R. Kumar, "Printed machine learning classifiers", in *MICRO '20*, **IEEE Top Picks Honorable Mention**.

[9] **N. Bleier**, M. H. Mubarik, F. Rasheed, J. Aghassi-Hagmann, M. B. Tahoori, and R. Kumar, "Printed microprocessors", in *ISCA '20*, **Selected for retrospective of the years 1996 through 2020 on the 50th anniversary of ISCA.**

Awards and Honors

- ISCA 25 Year Retrospective Selection *Printed Microprocessors* 2023
- ISCA '23 Best Paper Nominee *Programmable Olfactory Computing* 2023
- Heidelberg Laureate Forum Invitee 2023
- IEEE Top Picks Honorable Mention *Printed Machine Learning Classifiers* 2020
- Min Wang and Pi-yu Chung Endowed Research Award 2022–2023
- Boeing Scholarship Fall 2022–Spring 2023
- Lieutenant General Thomas M. Rienzi Graduate Award 2019–2020

- Bronze Star Medal, Afghanistan Campaign Medal with Campaign Star, Army Commendation Medal, Combat Infantryman Badge, Ranger Badge, Airborne Badge 2008–2014

Teaching

- **Advanced VLSI System Design (ECE 498HK)** Co-Instructor — Fall 2023
  Set-up environment and workflow for 65 nm *VLSI process. Taught undergraduate students how to perform synthesis, place-and-route, DRC, etc. using Cadence and Synopsys tools. Course resulted in multiple succesful tape-outs and bring-ups.*
- **Computer Organization and Design (ECE 411)** Teaching Assistant — Fall 2019 –Fall 2020
  Designed and implemented an autograder for course machine problems. Machine problems include design and verification of a pipelined RISC-V microprocessor. Designed and implemented a TA lead discussion series. Gave lectures on Tomasulo algorithm and O3 architectures.
- **Computer Architecture (ECE 511)** Teaching Assistant — Spring 2019
  Designed and implemented a machine problem consisting of design and formal verification of several cache coherence protocols.
- **Concepts in Engineering Mathematics (ECE 298JA)** Teaching Assistant — Fall 2017
  Taught sections on mathematics relevant to electrical engineering. Topics included Fourier analysis, complex analysis, and elementary number theory.

Students Mentored

- **Ramakrishna Kanungo** 2nd year Masters student
  Microarchitecture design and chip tapeout. Secured industry job in load-store unit design.
- **Stanley Wu** 1st year PhD student
  Stochastic programming via multistage optimization for economic forecasting in uncertain supply and demand scenarios.
- **Abigail Wezelis** 2nd year Masters student
  PERF and custom (PIN) based application performance modeling on commodity and microcontroller class systems. Secured industry job in embedded system design.
- **Srijan Chakraborty** 2nd year Masters student
  Synthesis and performance/area/power analysis of very large RTL designs.
- **Calvin Lee** Undergraduate student
  Assembly programming and assembler design and implementation. Calvin is now a graduate student at Stanford.
- **Joseph Ravichandran** Undergraduate student
  Implementation of custom synthesis passes in Yosys. Joseph is now a PhD student at MIT.
- **Ian Dailis** Undergraduate student
  Implementation of ASIC design flow including a customized automatic place & route algorithm for pseudo-CMOS logic implemented with organic transistors. Ian has succesfully taped-out a microprocessor using this design flow.

Education

University of Illinois at Urbana-Champaign Urbana, IL
Ph.D. Candidate in Electrical and Computer Engineering, Advisor: Rakesh Kumar 2019–Current

University of Illinois at Urbana-Champaign Urbana, IL
B.S. in Electrical and Computer Engineering 2016–2018

Grant Proposals

- **Earable and Olfactory Computer Systems: Benchmarks, Architectures, and Chip Implementations** NSF Small

- **Making Analog Side Channels a First-Class Consideration in Architecture-Level Design** NSF Medium

References

- **Rakesh Kumar**
  Professor and John Bardeen Faculty Scholar
  Department of Electrical and Computer Engineering
  University of Illinois at Urbana-Champaign.
- **Josep Torrellas**
  Saburo Muroga Professor
  Department of Computer Science
  University of Illinois at Urbana-Champaign
- **Pavan Hanumolu**
  Seendripu Family Professor
  Department of Electrical and Computer Engineering
  University of Illinois at Urbana-Champaign
- **Trevor Mudge**
  Bredt Family Professor
  Department of Computer Science and Engineering
  University of Michigan
- **Nam Sung Kim**
  Sanders III - AMD, Inc. Endowed Chair Professor
  Department of Electrical and Computer Engineering
  University of Illinois at Urbana-Champaign